CLAIMS:

1. A circuit arrangement for converting a preferably analog input signal from at least a receiver, particularly at least a UHF or VHF receiver, into a digital output signal, said circuit arrangement (100) comprising:

at least one threshold value circuit (30) having a first input (32) for receiving the input signal;

a second input (34) for receiving a reference threshold signal generated by at least one reference threshold signal detector (20); and an output (36),

the digital output signal being formed in the threshold value circuit (30) by comparing the input signal at the first input (32) with the reference threshold signal at the second input (34);

at least one detector circuit (40) arranged subsequent to and communicating with the threshold value circuit (30) for detecting overshoots and/or pauses and/or interruptions in the input signal; and

at least one control circuit (50) communicating with the detector circuit (40) and the reference threshold signal detector (20), the output signal of said control circuit ensuring that the reference threshold signal applied to the threshold value circuit (30) during time intervals (T_{aus}) that are assignable to the overshoots and/or the pauses and/or the interruptions detected by the detector circuit (40) is maintained at approximately the reference threshold value comprising the reference threshold signal at the start of the overshoot and/or the pause and/or the interruption,

characterized in that

the reference threshold signal detector (20) forms the reference threshold signal from the input signal and comprises at least a resistor (22) having a variable resistance value (R) and at least a capacitive element (24) having a capacitance (C) arranged subsequent to the resistor (22), and in that

the resistor (22) assumes a high-ohmic state preventing a discharge of the capacitive element (24) during the time intervals (T_{aus}) that are assignable to the overshoots and/or the pauses and/or the interruptions, and a low-ohmic state during the time intervals that are not assignable to the overshoots and/or the pauses and/or the interruptions.

2. A circuit arrangement as claimed in claim 1, characterized in that the input signal is present in the form of a low-frequency analog baseband signal converted in the receiver.

3. A circuit arrangement as claimed in claim 1 or 2, characterized in that the first input (32) of the threshold value circuit (30) is preceded by at least a filter stage (10).

4. A circuit arrangement as claimed in any one of claims 1 to 3, characterized in that the threshold level of the reference threshold signal adapts to the level of the input signal in the low-ohmic state of the resistor (22).

5. A circuit arrangement as claimed in any one of claims 1 to 4, characterized in that the threshold value circuit (30) is constituted by a comparator whose first input (32) is positive and whose second input (34) is negative.

6. A circuit arrangement as claimed in any one of claims 1 to 5, characterized in that the detector circuit (40) comprises at least a slope detector unit (42) and at least a clock regaining unit (44) connected to the slope detector unit (42), and in that the detector circuit (40) regenerates the data clock (f_{data}) from the digital output signal.

7. A circuit arrangement as claimed in claim 6, characterized in that the control circuit (50) comprises at least a decision unit connected to the slope detector unit (42) and the clock regaining unit (44), whose respective outgoing signals change the resistor (22) either to the high-ohmic state or to the low-ohmic state.

8. A circuit arrangement as claimed in any one of claims 1 to 7, characterized in that the control circuit (50) has an externally and/or internally triggerable reset function.

9. A circuit arrangement as claimed in claim 8, characterized in that, after triggering the reset function of the control circuit (50), the resistor (22) assumes the low-ohmic state.

10. A circuit arrangement as claimed in claim 8 or 9, characterized in that, after triggering the reset function of the control circuit (50), the capacitive element (24) is chargeable to a given capacitance (C_t).

11. A circuit arrangement as claimed in any one of claims 1 to 10, characterized in that the capacitive element (24) is constituted at least as a capacitor.

12. A circuit arrangement as claimed in any one of claims 1 to 11, characterized in that an additional, fixed reference value is adjustable at the second input (34) of the threshold value circuit (30), particularly by means of an additional resistor.

13. A receiver, particularly a UHF or VHF receiver, comprising at least a subsequent circuit arrangement (100) as claimed in any one of claims 1 to 12.